Latchup in CMOS Analog-to-Digital Converters†

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Abstract *- Heavy-ion latchup is investigated for analog-to-digital converters. Differences in cross section for various ions shows that charge is collected at depths beyond 50 μm, causing the cross section to be underestimated unless long-range ions are used. Current distributions and thermal imaging were used to identify latchup-sensitive regions. Latchup in one of the circuit types was catastrophic, even when the power was turned off within 10 ms of a latchup event.*

I. INTRODUCTION

Many CMOS circuits are sensitive to latchup from heavy ions, and latchup is one of the major considerations when CMOS devices are evaluated for space applications. Radiation-induced latchup has been studied for many years [1-8], but it remains a difficult problem in actual circuits because latchup sensitivity inherently depends on the layout and distribution of contacts, power and ground within complex circuits [9].

Commercial CMOS devices are designed to withstand electrically induced latchup from transients or start-up conditions at the input, output and power supply connections, but generally do not consider triggering from *internal* transients such as those caused by heavy ions. Many CMOS devices are fabricated on so-called epitaxial substrates where a relatively thin lightly doped epitaxial region is grown over a highly doped, low resistivity substrate. Although epitaxial substrates do not necessarily eliminate latchup from heavy ions or protons in space, the increasing trend towards epitaxial construction has generally improved latchup performance in space environments.

High-performance analog-to-digital converters are an exception. They are usually designed with bulk substrates because epitaxial substrates induce approximately three times more noise from the digital to the analog region [10]. Thus, latchup is a critical issue for A-D converters. This paper discusses latchup in two types of converters from one manufacturer. Both converters are sensitive to latchup from heavy ions. Although it does not always occur, many of the latchup events cause catastrophic failure in these devices. Catastrophic failure is a difficult problem to address. In some cases catastrophic failure can be masked by circuit issues during testing that inadvertently prevent the latchup event from progressing to the point where catastrophic failure occurs.

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II. EXPERIMENTAL APPROACH

The Analog Devices AD9240 is a successive-approximation 14-bit analog-to-digital converter that incorporates three different power supply connections (all 5 V). The maximum conversion rate is 10 Mb/s. One supply is used for the analog section of the part, and it has the highest power consumption during normal operating (nominally 50 mA). A second power supply connection is used for digital circuitry in the *interior* regions of the digital part of the chip, and it typically requires about 7 mA during normal operation. A third power supply is used to provide power to the output drivers. The nominal current is only a few mA, depending on duty cycle and output loading.

The AD9260 is a 16-bit sigma-delta oversampling converter with a pipeline technology that provides high conversion rates. The AD9260 also uses three 5-V power supplies, just as for the AD9240. When operating at the maximum conversion rate (20 megasamples per second clock rate), the total power consumption is 550 mW. Most of the power is consumed in the analog portion of the chip.

Both converters are only available in plastic packages. A special acid delidding system was used to etch away the plastic at the top surface, thereby allowing direct access to the top of the die for heavy-ion testing. For radiation tests, the devices were mounted in evaluation boards, provided as a standard item by the manufacturer for evaluation purposes. The evaluation boards are designed to minimize electrical noise and interference between the digital and analog sections of the device, and provide a far less costly alternative compared to the development of custom test fixtures.

Radiation testing was done by irradiating the device in the test board, monitoring functional operation and the currents in each power supply. A special power supply was used that could shut down power within about 10 ms after a high-current condition was found in any of the power supplies. The current trigger conditions and current limit could be programmed separately. Rapid shutdown prevented destructive burnout for the AD9240 and minimized heating during the time that latchup occurred. However, the shutdown procedure was not effective for the AD9260; catastrophic failure occurred approximately 30% of the time.

Radiation tests were done at two different accelerators. Most of the tests were done at Brookhaven National Laboratory, which provides ions with more limited range (typically 30 to 45 μm, depending on the ion type). Some tests were done at Texas A$M, where ions are available with ranges well above 100 μm. Additional tests were done with californium-252 because of the low cost and convenience, and ease of studying specific latchup paths.

III. Test and Characterization Results

A. *Heavy Ion Test Results - AD9240*

The cross section for latchup of the AD9240 is shown in Figure 1. Data were obtained from several different experiments, some of which were done at angle to increase the effective LET. The effective range (taking the incident angle into account) is shown for each data point. Counting statistics are nominally 5-8%. Note that the cross section is substantially higher for ions with longer range; in particular the cross section for the last data point with 23 μm range is about a factor of three lower than that of the next-to-last data point that was taken with a 160 μm range ion. The threshold LET was above 15 MeV-cm^2/mg. This difference in range is consistent with charge collection in bulk substrate devices (see Dodd, et al.[11]).

The cross section increases somewhat gradually over a wide range of LET values. All of the tests with heavy ions were done using somewhat conservative current limit values for the three power supplies to avoid destroying the device, and to allow a series of tests to be done on a small number of devices. The current limit values were 30 mA for the two digital power supplies (with nominal operating values of 2 to 7 mA) and 100 mA for the analog power supply (with nominal operating current 50 mA). The equilibrium current condition approximately 100 ms after latchup occurred was monitored for each latchup event. Although many

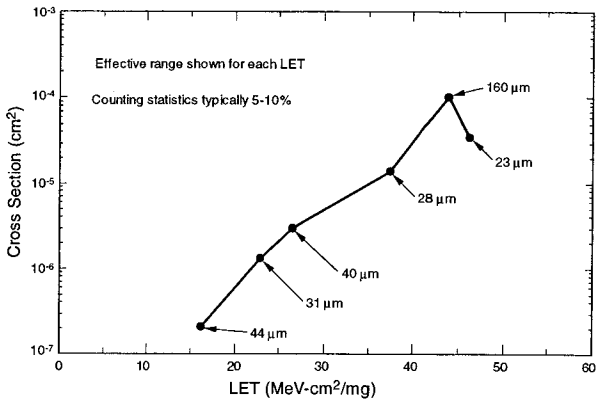

Figure 1. Latchup cross section of the Analog Devices AD9240 obtained after several different radiation tests. Note the different ranges for various points on this curve.

of the events corresponded to full current limit for the analog power supply (100 mA), about 25% of the events resulted in an equilibrium current below that limit.

Later tests were done using californium ions in our laboratory with the current limit of all three power supplies extended to 2 A. Those tests provided better information about the equilibrium currents in typical applications where there are relatively large capacitors that can provide much higher currents compared to the restricted current from the special power supply system used for the heavy ion tests. The tests done with broader current limit control showed a very wide range of latchup equilibrium currents for the digital power supply, ranging from about 45 to more than 300 mA. A histogram of the currents obtained during the tests with californium is shown in Figure 2. Similar variability occurred for currents in the analog power supply for latchup events that caused current to increase in the analog circuitry.

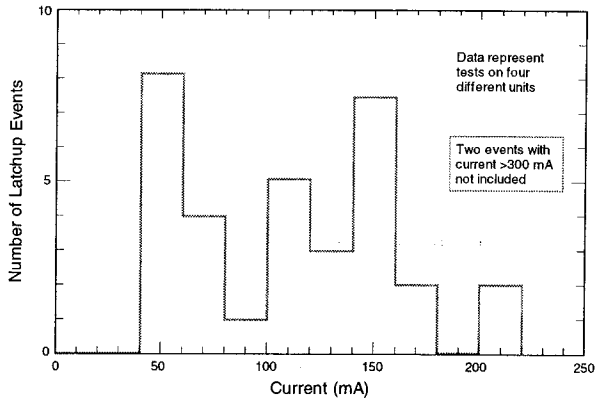

Figure 2. Histogram of many different latchup events showing the wide range of equilibrium currents in the digital power supply when the devices were irradiated (and latched) with californium. Power supply current limiting (2 A) was well above the highest latchup current

The latchup events with californium were of two types, as determined by monitoring the power supply currents. Latchup occurred either in the interior digital regions or the analog section, but never in the output drivers. Most of the latchups did not result in device destruction, even though the current limit was 2 A. Note however that ^{252}Cf is not necessarily capable of triggering events that correspond to LET above about 25 MeV-cm^2/mg because of the limited range of the californium fission fragments.

Some tests were done by leaving the device in a latched state, allowing subsequent latchup events to occur. Substantial heating of the device occurred after the first latchup event, allowing later latchup events to be more easily triggered. Figure 3 shows a representative test of this type in which four latchup events were observed in the analog region of the device. Note that the current drops slightly after each current "step," probably because the metallization resistance and well resistance increase due to localized heating. The last event resulted in destructive failure of the device.

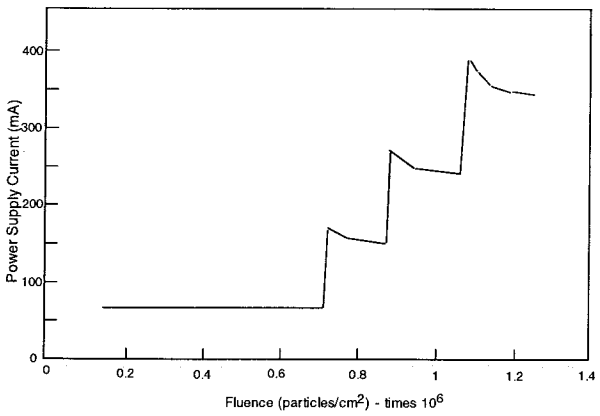

Figure 3. Sequence of latchup events during tests with continual irradiation with californium fission fragments. Each current step corresponds to an additional latchup event in a different region of the device.

B. Thermal Imaging of Latched Regions

It is very difficult to determine which internal regions of complex devices are actually involved in the latchup path, particularly for devices with extensive metallization coverage that preclude the use of lasers. We used a thermal imaging system, coupled through an infrared microscope, to examine the surface of devices after latchup. The system contains software for automated analysis of the temperature distribution. However, the calibration is limited by the variation in thermal emissivity in different regions (areas covered by metallization have lower emissivity than silicon regions of the chip).

Higher sensitivity (and better thermal accuracy) can be obtained by coating the device after latchup has occurred with a thin layer of black paint to provide more uniform emissivity. The paint layer was applied after latchup in order to avoid interposing material between the surface of the device and the californium ions (the thickness of the paint is not very well controlled). After the initial image was taken (with the device latched), power was momentarily interrupted and the device was allowed to come to thermal equilibrium for about two minutes. At that time a second thermal image was taken. The difference between those two images was then used to measure the actual surface temperature of the device, assuming an emissivity near one. The thermal imaging system is calibrated to read temperature in this way. Surface temperatures of about 130 C were measured, as shown in Figure 4. Note that the hot region is confined to a very small region, and that temperatures below the surface are very likely at a much higher temperature compared to the temperature at the surface.

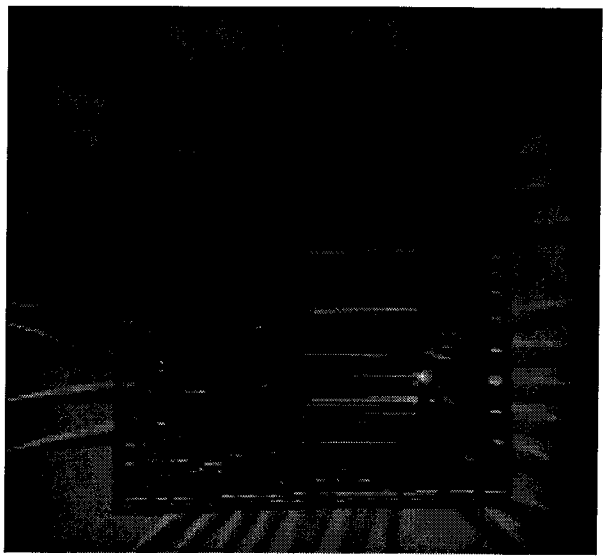

Figure 4. Example of differential thermal image showing the presence of a small latchup region in the analog region of the AD9240.

Many regions of the AD9240 were sensitive to latchup. Figure 5 shows an outline of the die, along with regions where latchup was observed during several different irradiations with californium. After each latchup event, the device was removed from the vacuum chamber (retaining power to keep the device in a latched condition) so that the thermal

imaging results correspond to equilibrium conditions with the device in air. The size of the heated regions was on the order of 15 to 30 μm in diameter.

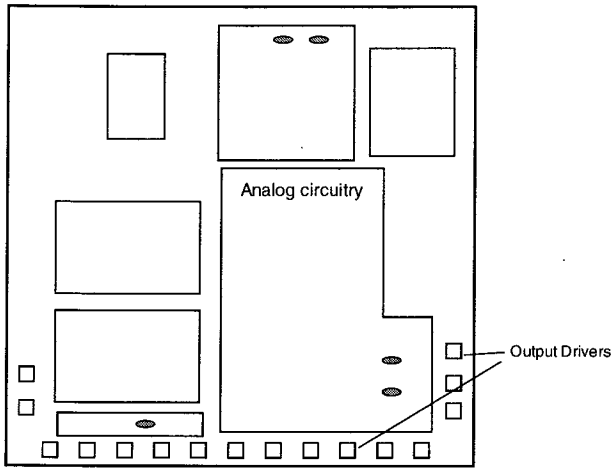

Figure 5. AD9240 latchup regions, determined by thermal imaging after tests with californium. Thermal imaging was not done during accelerator tests because of the cost for the "dead" time required to continually interrupt radiation testing to do the thermal imaging.

Snapback [12,13] can also cause circuit malfunctions when devices are irradiated with heavy ions, and snapback has many similarities to latchup. Generally the current involved in snapback is much lower because it involves only current *within* a single MOS transistor and does not involve large currents in the substrate. The magnitude of the currents observed in our tests along with the thermal signature observed with thermal imaging support the conclusion that these events are due to latchup, not snapback.

C. *Heavy Ion Results for AD9260*

Although the fabrication process is essentially the same for the AD9260 as for the AD9240, most of the latchup events in the AD9260 were catastrophic. Consequently it was only possible to get latchup results with the power supply current limit set very closely to the normal power supply current. Most of the latchup events in the AD9260 occurred in the analog power supply. Figure 6 shows a histogram of equilibrium voltages where the current increases from a nominal 70 mA to 90 mA during latchup. The distribution of voltages provides an approximate measure of the distribution of latchup sites within the device (a similar plot for the AD9240 shows a much wider distribution of equilibrium voltages).

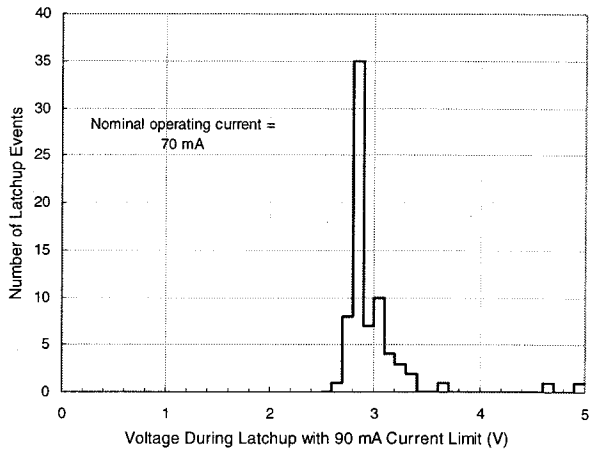

Figure 6. Histogram of equilibrium voltages for the AD9260 with the current limit set close to the nominal operating current.

The threshold LET for the AD9260 was 7.9 MeV-cm^2/mg, nearly a factor of two lower than that of the AD9240. The cross section was 5.1 x 10^{-7}; it increased to about 7 x 10^{-6} at an LET of 11.1 MeV-cm^2/mg. The destructive nature of the latchup events prevented us from completely characterizing the latchup cross section.

IV. Discussion

A. *General Considerations*

Latchup in these analog-to-digital converters shows the complexity of latchup in modern devices. A number of issues have to be considered.

First, for devices with bulk substrates it is essential that the effective range of the ions used for testing is above 40 μm because charge collection occurs deep within the substrate. If ions with shorter range are used the cross section will be too low. It is also possible to overestimate the threshold LET value by a considerable amount because the latchup threshold will be higher for short range ions due to the decreased charge deposition. This can introduce significant errors in estimating latchup failure rates in space applications.

Second, current limiting has to be used very cautiously when latchup tests are done. If the current limit is too low it may prevent some latchup events from occurring, underestimating the cross section and causing catastrophic latchup to be missed. For the AD9240, current limiting of the digital power supply caused the analog section to be loaded down when latchup occurred in the digital region, erroneously indicating that all latchup events occurred in the analog region of the circuit. Subsequent tests with higher current limits showed that latchup could occur in digital as well as analog regions of the devices.

Third, many different internal regions can latch, and it is necessary to observe very large numbers of latchup events with several different types of ions in order to get the proper picture of how latchup affects different regions of the part. Using power supply current detection and shutdown as a circumvention method is difficult for a device of this type because of the large number of different latchup paths that are present in the circuit along with the wide range of currents that occur for different latchup paths. It is necessary to monitor all power supplies and to consider variations in nominal operating current for different units and operating conditions in order to establish detection limits.

B. Temperature Sensitivity

Threshold LET and cross section are both sensitive to temperature, as shown in Figure 7. Although one might expect that this is due to the dependence of transistor gain on temperature, that factor turns out to be unimportant because the four-layer structure involved in latchup contains internal paths that effectively shunt the base-emitter region of both transistors. This causes the effective gain of the structure to be much lower than the gain with an open base. The dominant reasons for the temperature dependence are first, temperature sensitivity of the well resistance; and second, the negative temperature coefficient of the forward voltage, V_{BE}[14]. For doping levels $< 5 \times 10^{17}/cm^2$, the well resistance doubles at 125 °C compare to room temperature. V_{BE} decreases 2 mV/°C, reducing the forward drop required across the isolation well for the vertical parasitic transistor, as well as the forward drop required in the substrate to forward bias the lateral transistor.

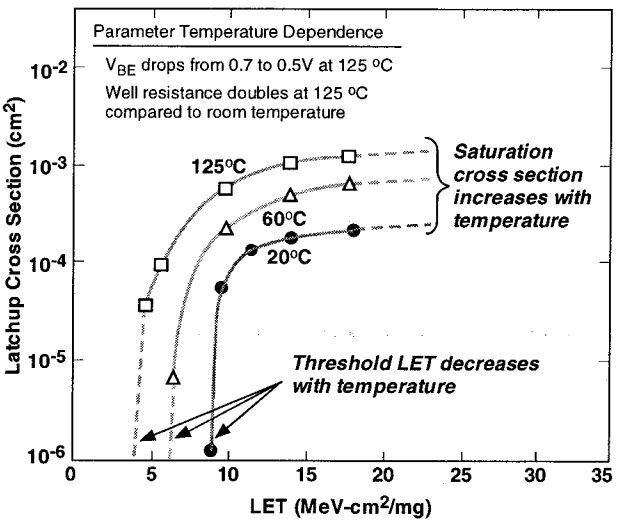

Figure 7. Dependence of latchup cross section on temperature for a CMOS device fabricated with a bulk process.

The temperature dependence of latchup is so high that it is necessary to derate test data taken at room temperature to account for the higher chip operating temperature that is typical of most space applications. A typical circuit board for spacecraft incorporates thin metallic plates to conduct heat from various devices on the board to the case or other region with large thermal mass. Consequently, chip operating temperatures are typically about 20 °C above the external case temperature. That rather small temperature difference will decrease the threshold LET to 70% of the value measured at room temperature, and will increase the cross section by factors of 2 to 3. The higher temperature may also change the equilibrium currents as well as the amount of heating that occurs in metallization.

It is also possible to use the temperature sensitivity of latchup as a diagnostic tool to determine whether the high-current condition is due to latchup, or to other mechanisms. Koga, et al. used that approach to determine that latchup -like characteristics in a bipolar device were actually caused by second breakdown, not latchup. Second breakdown changes very little with temperature.

C. Catastrophic Failure Mechanisms

Relatively little attention has been given to determining the underlying reasons for catastrophic failure from latchup. One reason is that latchup is often used as a "go/no go" factor for using parts in space. If ground tests show that a device is sensitive to latchup, usually it is eliminated from further consideration. That is particularly true for devices that exhibit catastrophic failure.

Another factor relates to the way that latchup testing is done. Tests at high accelerators are costly, and nearly always require that the device is placed in a vacuum chamber at the exit port of the accelerator. If a devices fails catastrophically, considerable time is required to open the chamber and pump it down after the device is changed. The goal of testing is usually to measure enough latchup events to determine the cross section. This cannot be done very easily if parts have to be continually changed because they are failing.

Latchup tests are usually done with special power control systems that sense the high-current condition just after it occurs, and shut down the power system a shortly thereafter. Consequently the only catastrophic failure modes that will occur are those which involve currents that pass through the latched region for short time periods. Although it is possible to leave the device in a latched state, this is awkward and costly at accelerator facilities because of the high cost of beam time. When this is done, it is usually possible to investigate only a small

number of conditions and current paths. Thus, attempts to determine catastrophic failure during tests at radiation facilities are usually of limited value.

Latchup causes a great deal of local heating within the sensitive region. However, unless the temperature is extremely high (> 500 °C) it is unlikely that latchup will affect semiconductor, oxide or contact regions during time periods of a few minutes or hours, even though high temperature rises for short times may affect long-term reliability.

The weakest regions of most devices are the metallization and the bond wires. We have found evidence of partial melting and recrystallization of metallization in some types of devices after catastrophic latchup has occurred, and there are other cases where the currents were high enough to destroy bond wire connections. However, in most cases there is no obvious "signature" for latchup failures that can be determined by simple examination of the top surface.

One reason may be that it is not always necessary to raise metallization temperature to the point where the metal actually melts. Murguia and Bernstein investigate pulsed metallization failure conditions using special test structures [16]. They determined that if the threshold current density was above approximately 10^5 A/cm^2, failure occurred at time periods below 1 μs. For lower current densities the current had to flow through the metallization for longer time periods, and there was an inverse relationship between current density and time. They developed a model to show that the failures corresponded to metallization temperatures of 280-350 °C, well below the melting temperature. The failures were caused by stress because of the difference in thermal expansion between the oxide layer under the metal and the passivation layer at the surface. The result was a microscopic crack in the metallization, causing it to be open. This mechanism is likely to occur during latchup as well, but the failures are difficult to detect by optical means because of the small size of the metallization crack. Other techniques, such as voltage contrast, may be useful in determining their location.

V. Conclusions

This paper has discussed latchup in two types of analog-to-digital converters. Analog-to-digital converters are unlikely to be fabricated on epitaxial substrates because of noise considerations, and thus latchup is likely to remain a critical issue for that category of circuit.

Even though these two devices are fabricated with the similar processes by the same manufacture, one of the device types exhibited catastrophic latchup even though the currents measured during latchup were estimated to be below 50 mA.

Latchup remains a very complex issue for applications in space. Latchup testing is made more difficult by the requirement for very long range ions, as well as the strong dependence of latchup on temperature. Thermal imaging was used as a diagnostic technique to show which regions of devices were sensitive to latchup and to estimate the surface temperature increase during latchup.

Although latchup mitigation techniques can sometimes be used for latchup-sensitive devices, considerable effort is required to ensure that these approaches are effective. The large number of latchup paths in modern circuits makes this approach particularly challenging.

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Introduction

Analog-to-Digital Converters

- Low power ADCs are typically fabricated with CMOS
- Bulk substrates preferred to reduce noise from digital section
- Increases likelihood of radiation-induced latchup

Latchup Involves Parasitic Bipolar Structures, Not MOS Transistors

- Complex process involving vertical transistor as well as lateral transistor
- Many different latchup paths are possible
- Well resistance and contact placement determine threshold conditions

Current in Latched Structures Is Highly Localized

- Power dissipation is highest near edge of well and substrate
- Lateral distances are typically 10-20 μm
- Current density is also high in metallization

Introductory slide summarizing basic features of latchup along with motivation for the study.

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Outline

Devices Selected for Study

Experimental Approach at Accelerators

Cross Section for Latchup

Special Diagnostic Methods Using Cf Source

Mechanisms for Catastrophic Failure

Conclusions

Outline of talk.

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Experimental Procedure

Two Types of ADCs Selected

- AD940 14-bit successive approximation converter
- AD960 16-bit sigma-delta converter
- Both devices use three power supplies: analog, digital, and I/O

Accelerator Facilities

- Brookhaven- relatively short range ions
- Texas A&M (ion range > 100 μm)
- Californium-252 (only for diagnostic tests)

Characterization Methods

- Measure current during latchup
- Power shutdown ~ 10 ms after latchup is detected
- Thermal imaging diagnostic tests

This slide discusses the types of ADCs that were used for the study, along with the test facilities and characterization methods.

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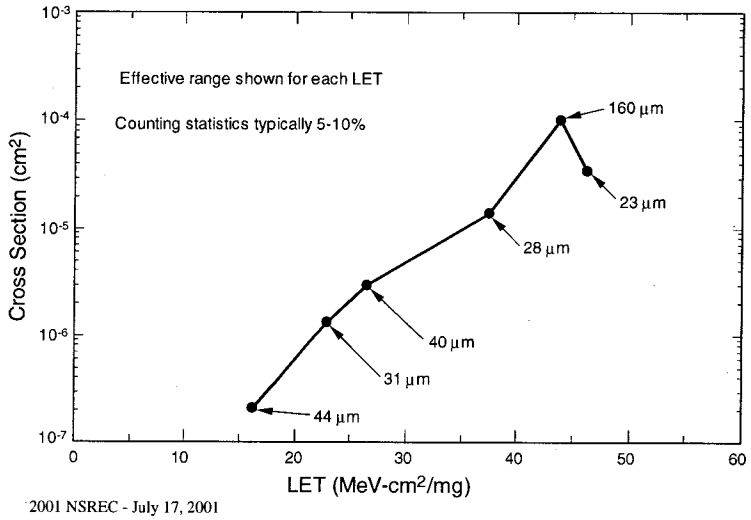
Latchup Cross Section for AD9240



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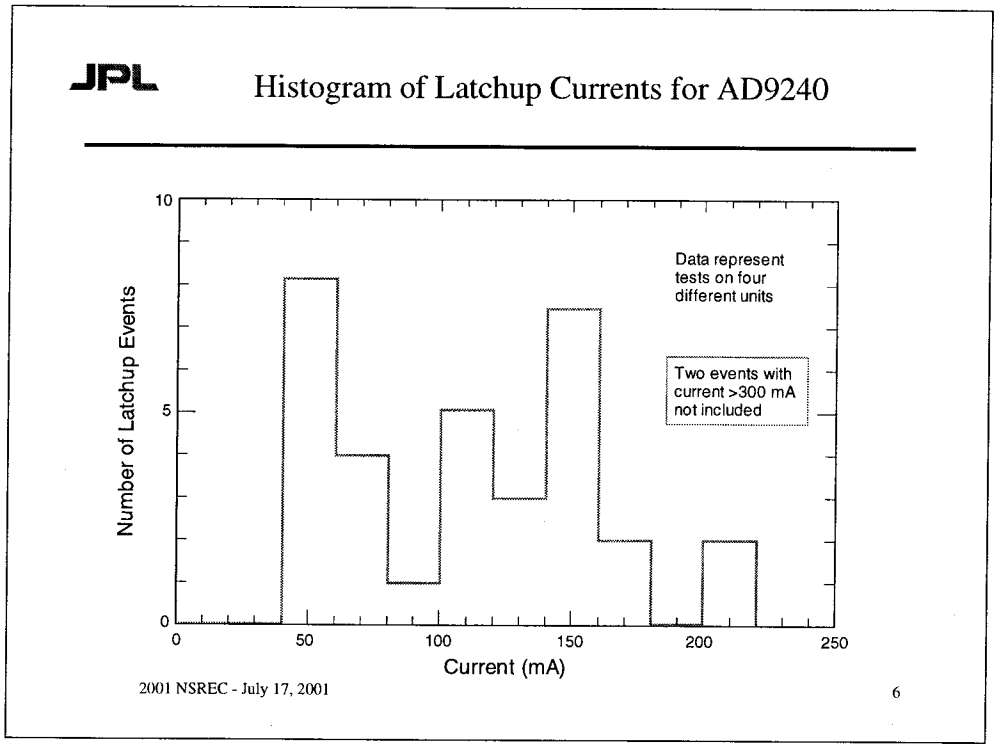
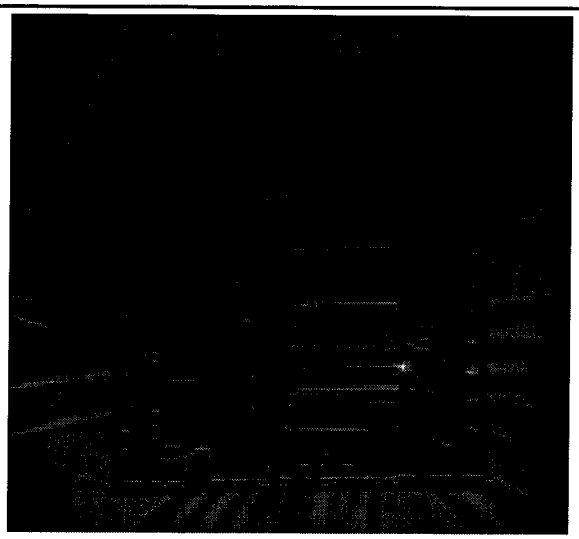
This slide shows the cross section for latchup that was measured for the AD9240. The cross section increases gradually as the LET increases. The large difference in cross section shown for the last two points illustrates the importance of using ions with long range for latchup testing.



This figure shows the distribution of currents that occur when a series of latchup events are recorded. The differences in current are due to the different locations of latchup paths within the circuit. Metallization resistance and holding voltage differ for the various paths. In this case, there is a particularly large difference in latchup currents because so many latchup paths are present in this circuit.

JPL Thermal Imaging Results for AD9240 Showing Extent of Latched Region



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This photo from a thermal imaging system shows the location of the internal heated region of an AD9240 that has been triggered into latchup by an energetic ion from Californium-252. After the latchup occurred, the device was coated with a thin layer of black paint to make the surface emissivity more uniform.

After the thermal image was recorded, power was temporarily removed to quench the latchup condition. A second thermal image of the normal device was then taken in order to establish a baseline for emissivity with the coat of black paint. The thermal imaging system software determined the surface temperature by analyzing the difference in the response of the two images.

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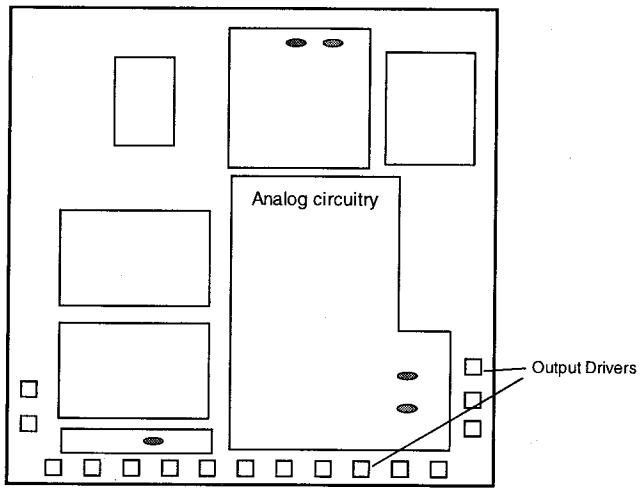
Latchup Sensitive Regions of the AD9240



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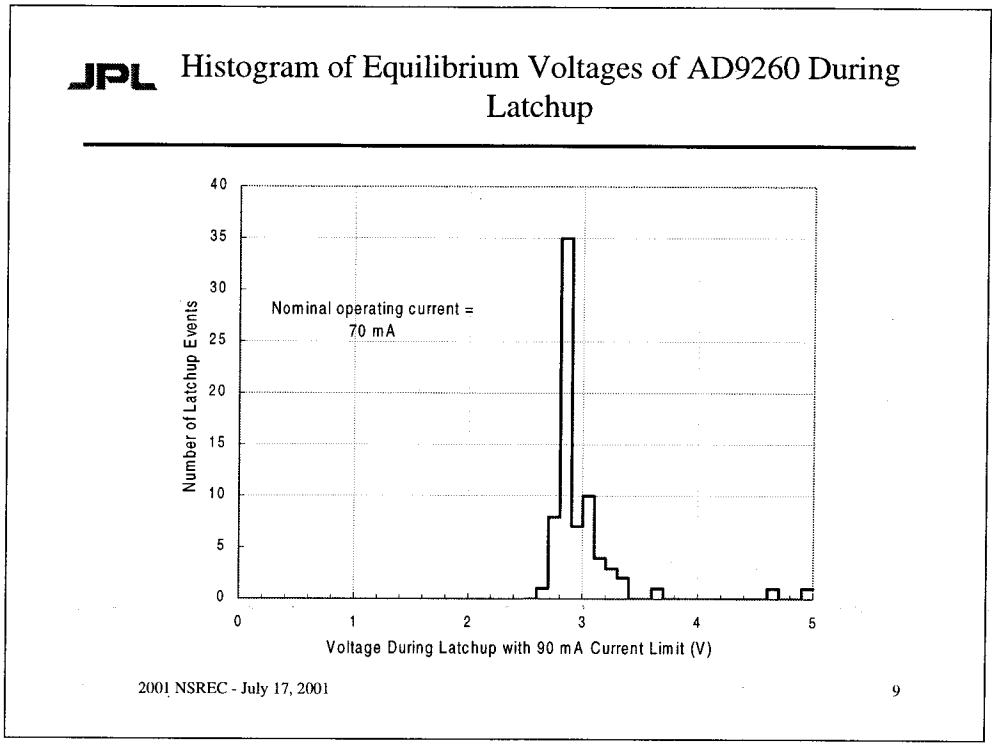
This slide shows various regions within the AD9240 that are sensitive to latchup. There are many more potential sites than shown in this diagram. The key point is that latchup paths occur in both the analog and digital regions of the circuit. There is an interplay between the digital and analog sections of the part that can create some confusion when latchup is being evaluated. Latchup events in the analog region can increase the current in the digital region if external current limiting causes the voltage in the analog section to decrease below 3 V.

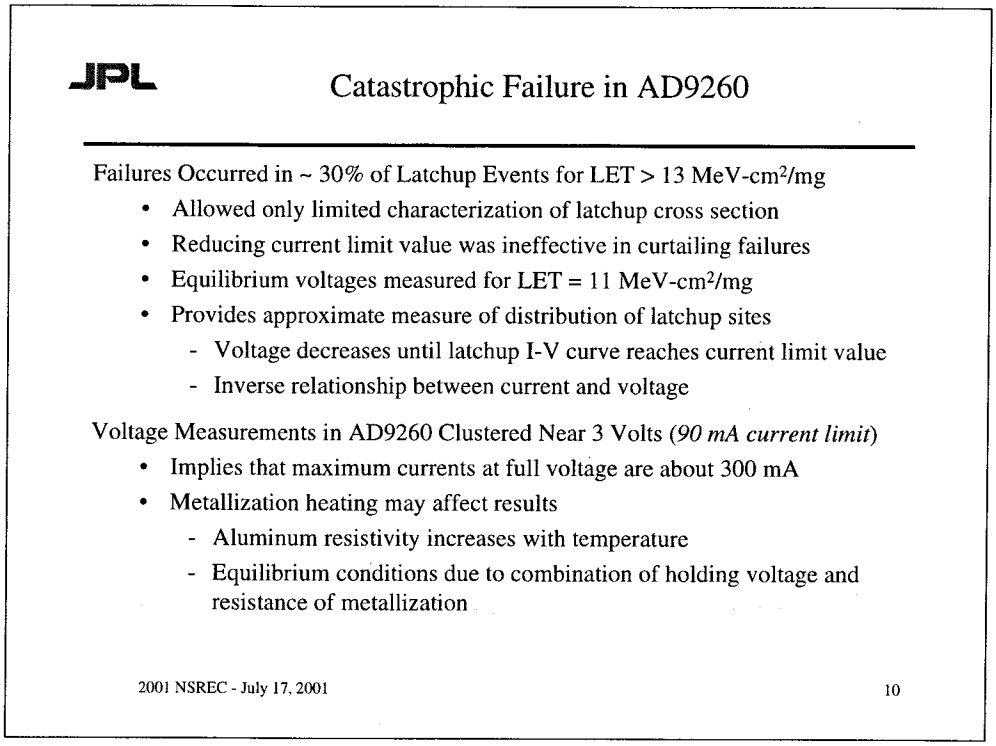
Interestingly, latchup was never observed in the input/output section of the device, possibly because the circuit design is intended to withstand electrical overshoot at those nodes.



This slide shows the distribution of latchup currents in the AD9260 at an LET of 11 MeV-cm^2/mg. Many of the latchup events at higher LET values were catastrophic, so this was the highest LET where a reasonable set of data could be obtained for this device.

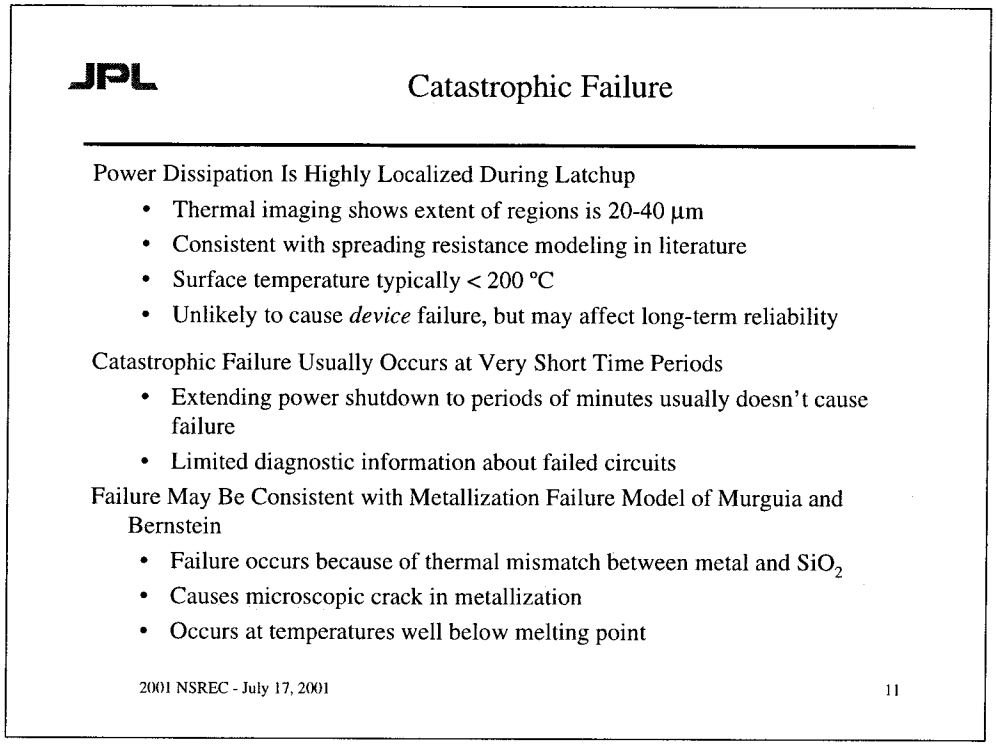
The current limit was set to 90 mA, with a normal operating current of about 70 mA. The small difference between the current limit and operating condition was necessary to avoid destructive latchup in this device.This distribution is quite narrow, implying that most of the latchup events are occurring in similar regions within the chip.

It is possible to estimate the current with 5 V applied by assuming a nominal holding voltage of 1.6 V.



For LET values > 13 MeV-cm^2/mg about 30% of the latchup events in the AD9260 were destructive. After a destructive failure the current in the device was lower than normal, and it would no longer operated correctly.

The catastrophic nature of the latchup events in this device prevented characterization of the latchup cross section, although it is possible to get a crude estimate from statistics of 2-3 devices.



Catastrophic failures are very difficult to analyze. Our thermal imaging results show that the temperature increase is highly localized and that the temperature appears to be too low for direct failure of the transistors or contacts. However, the localized thermal heating may affect longer term reliability.

The most likely failure mode is metallization. Murguia and Bernstein developed a model for metallization failure from short pulses which is caused by stress from the difference in thermal expansion coefficient of the metallization and the silicon dioxide regions above and below. Their work showed that such failures occur well below the melting point of aluminum, and typically produce a very narrow crack in the metallization that is difficult to detect through optical microscopy. For very high current densities the failure modes were independent of pulse width, which may explain why some latchup failures cannot be avoided by shortening the time period between latchup and power shutdown.

Reference: J. E. Murguia and J. B. Bernstein, "Short-Time Failure of Metal Interconnect Caused by Current Pulses," IEEE Elect. Dev. Lett., 14 (10), 481 (1993).

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Conclusions

Latchup Is a Key Problem for Low Power Analog-to-Digital Circuits

- Epitaxial substrates increase electrical noise, cost
- Performance features of commercial ADCs are required

Latchup Characterization Remains a Difficult Problem

- Many different latchup paths are present in most circuits
- Power dissipation is highly localized
  - Thermal imaging shows extent of heated regions
  - Catastrophic failure may occur at short times
  - Reliability may be affected in circuits without catastrophic failure

Other Issues

- Strong temperature dependence
- Variability between devices and production lots

Latchup is a particularly severe problem for low power analog-to-digital converters because of the difficulty of maintaining high resolution and accuracy on low-resistivity substrates. Consequently, commercial ADCs are nearly always fabricated on bulk substrates which increases the likelihood that they will be sensitive to latchup from heavy ions in space.

Characterization of latchup is a very difficult problem for these devices because there are so many different latchup paths, as well as separate power supplies for different regions of the circuit that may interact when latchup occurs in one section.

Catastrophic failure was observed in one of these devices even though it was fabricated with the same basic process as the other circuit. The catastrophic failures are most likely caused by metallization failure.

The strong dependence of latchup on temperature and the variability of latchup characteristics between different devices and production lots must be taken into account before latchup circumvention methods are used in space.